METAMAKO

Techniques for trading on FPGA enabled switches

Dr David Snowdon
CTO

Simplifying networks
Reducing latency in Electronic Trading
Opening up network packet visibility
Increasing flexibility

Basics

Basics — Who are Metamako?

METAMAKO

The leading vendor of high performance network devices for trading

Based in Australia, Global offices

Basics — Who are Metamako?

- Build a first class platform to host FPGA apps
  - Hardware (x86 + L1 + FPGA)
  - Network operating system
  - IP Cores
  - Containers

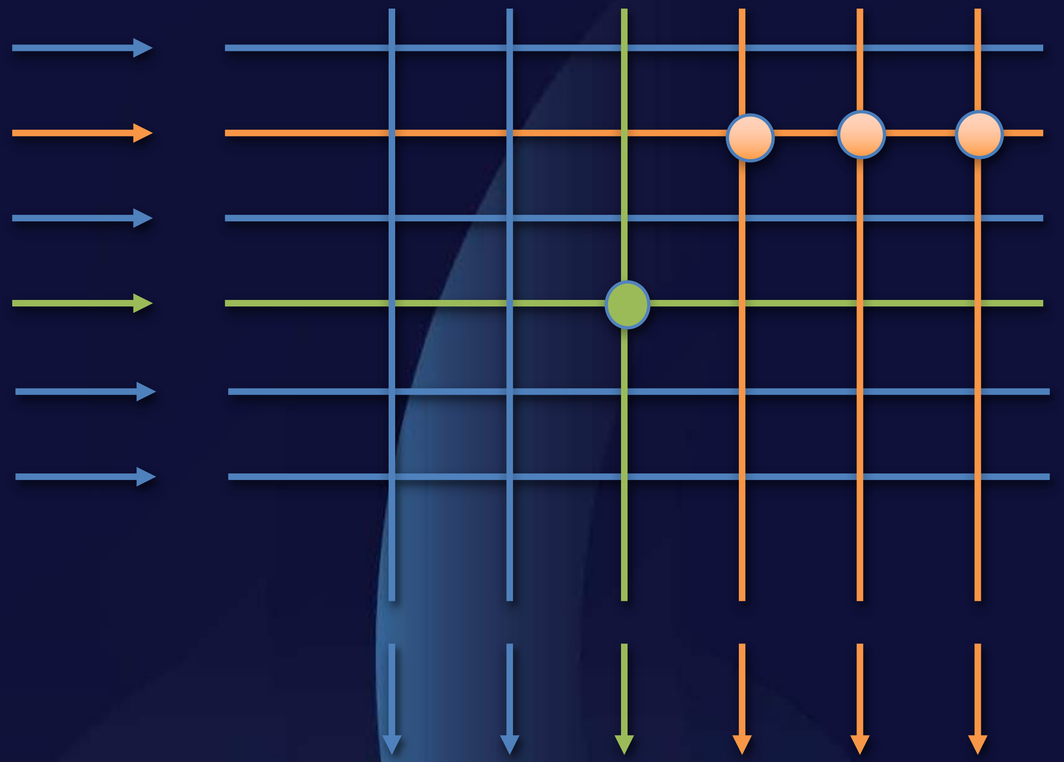
- Build our own FPGA apps to produce best-in-class devices
  - MetaWatch — Timestamping and packet capture
  - MetaMux — High performance exchange access

Basics — Who are Metamako?

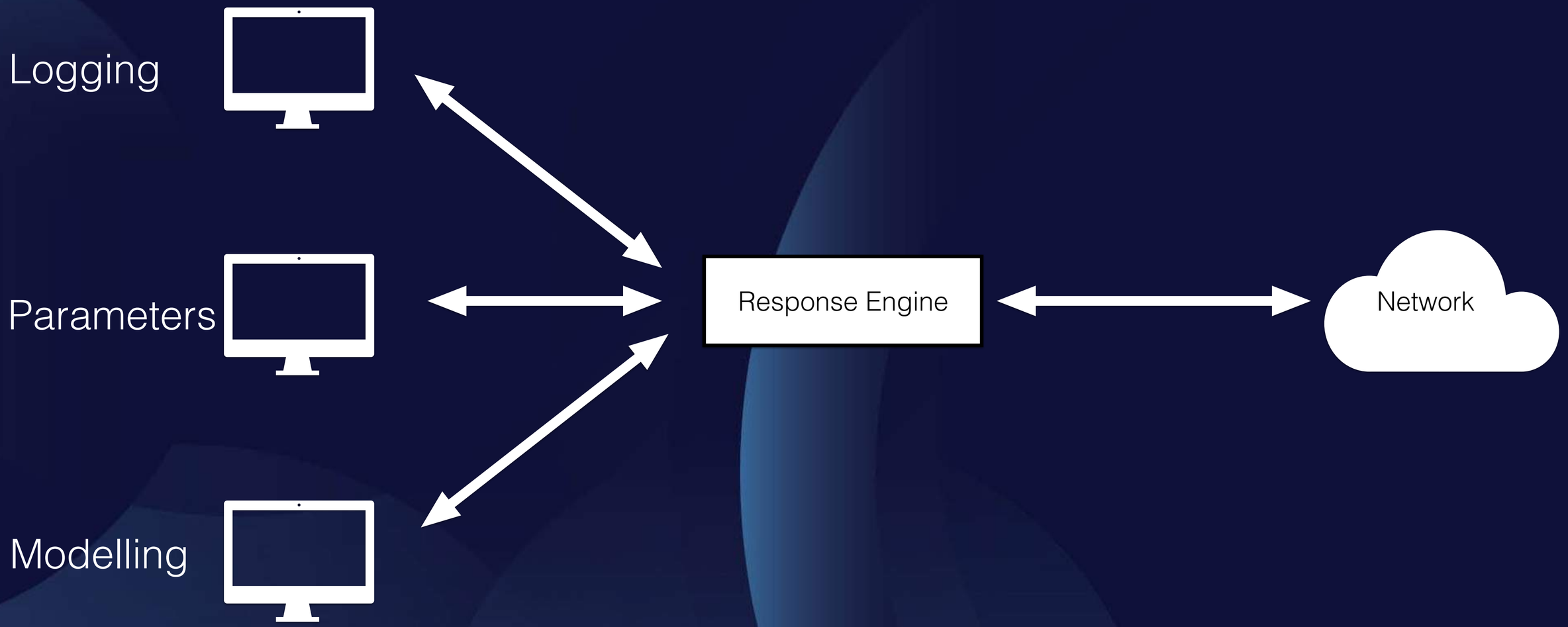
- MetaWatch
  - Cost effective network monitoring
  - 1 ns precision timing
  - Robust deep buffering (8GB)

Ideal for MIFID II RTS 25 Compliance

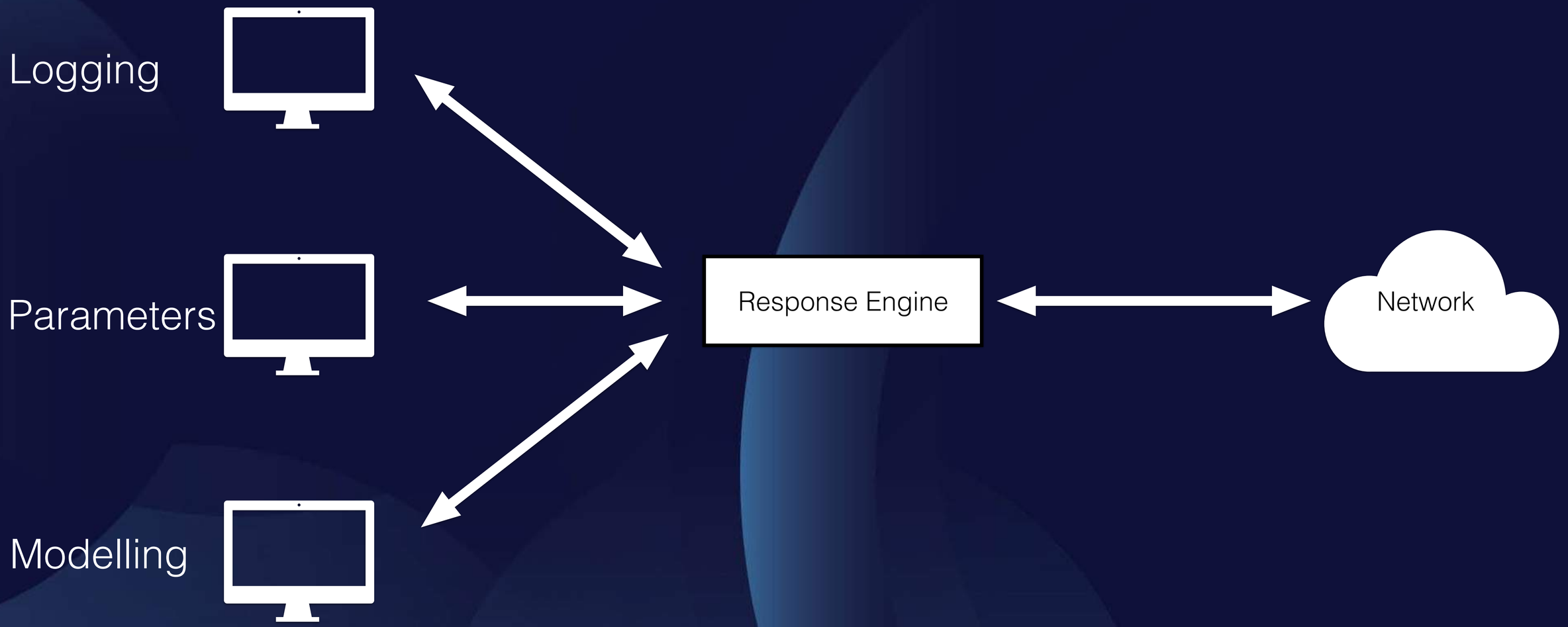
Basics — Layer 1 Switch



Basics — Software Trading Systems



Basics — FPGA Trading Systems



Basics — The advantages of FPGA

- Low latency
- Predictability/Determinism
- Performance

FPGA Platforms

FPGA Development Platforms

MetaApp 32

MetaMux 48

MetaConnect 96

FPGA Development Platforms

K-Series Devices Virtex 7	C-Series Devices Arria 10
	
MetaApp 32	MetaApp 32C
	
MetaMux 48K	MetaMux 48
	
MetaConnect 96K	MetaConnect 96C

FPGA Development Platforms

- Development kit, example designs, tips and tricks:

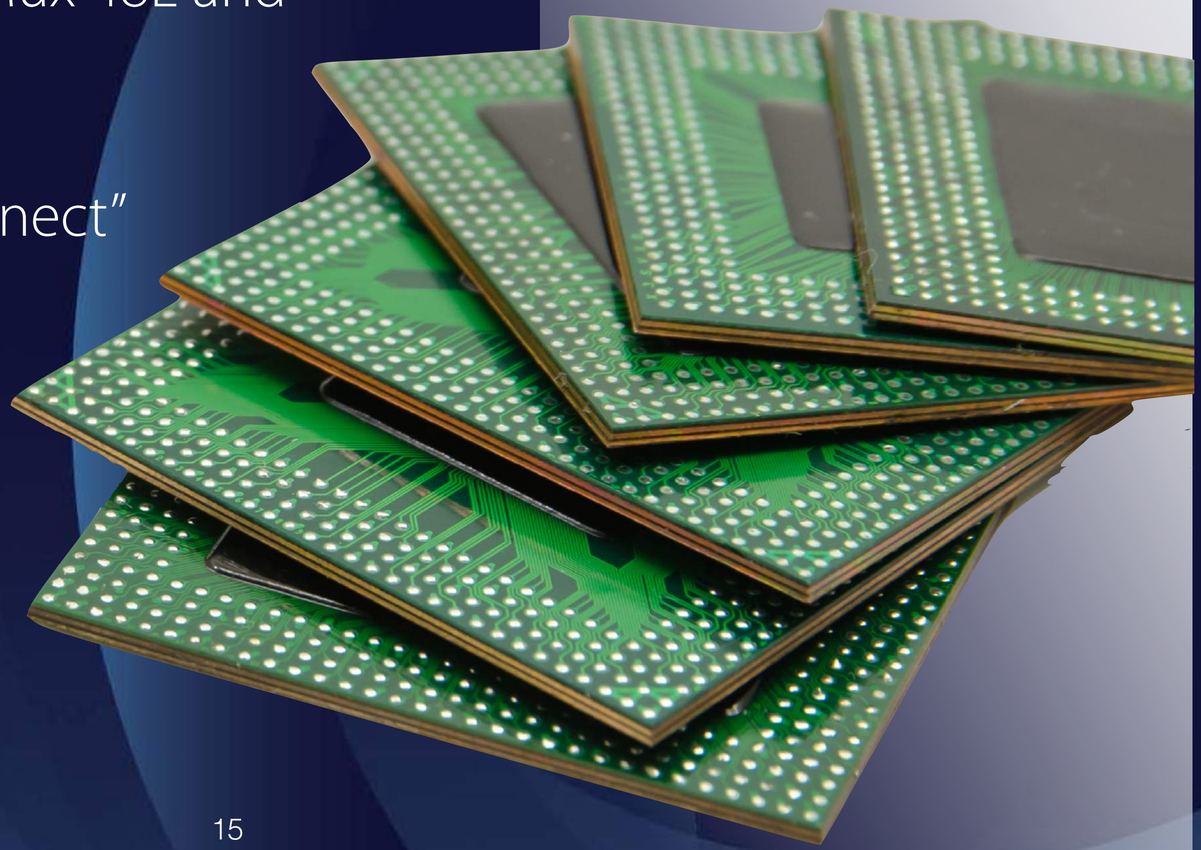
www.metamako.com/support

E-Series

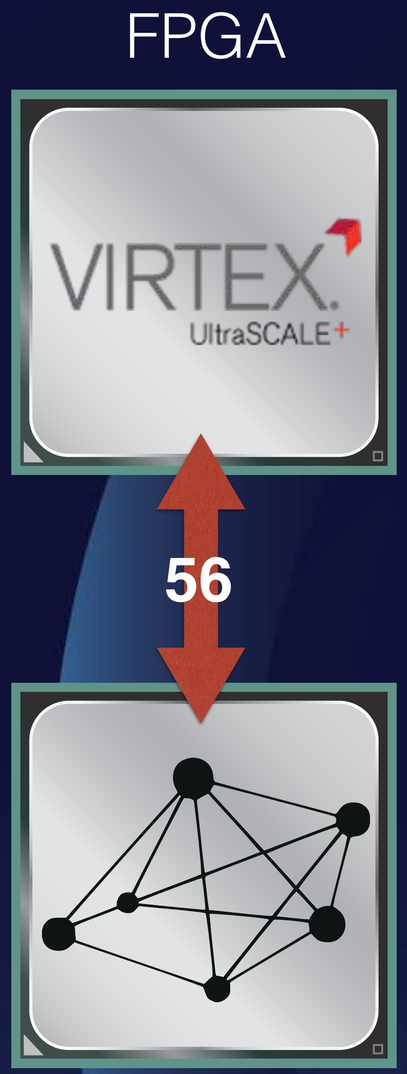
E-Series

XILINX
ALLIANCE PROGRAM
MEMBER

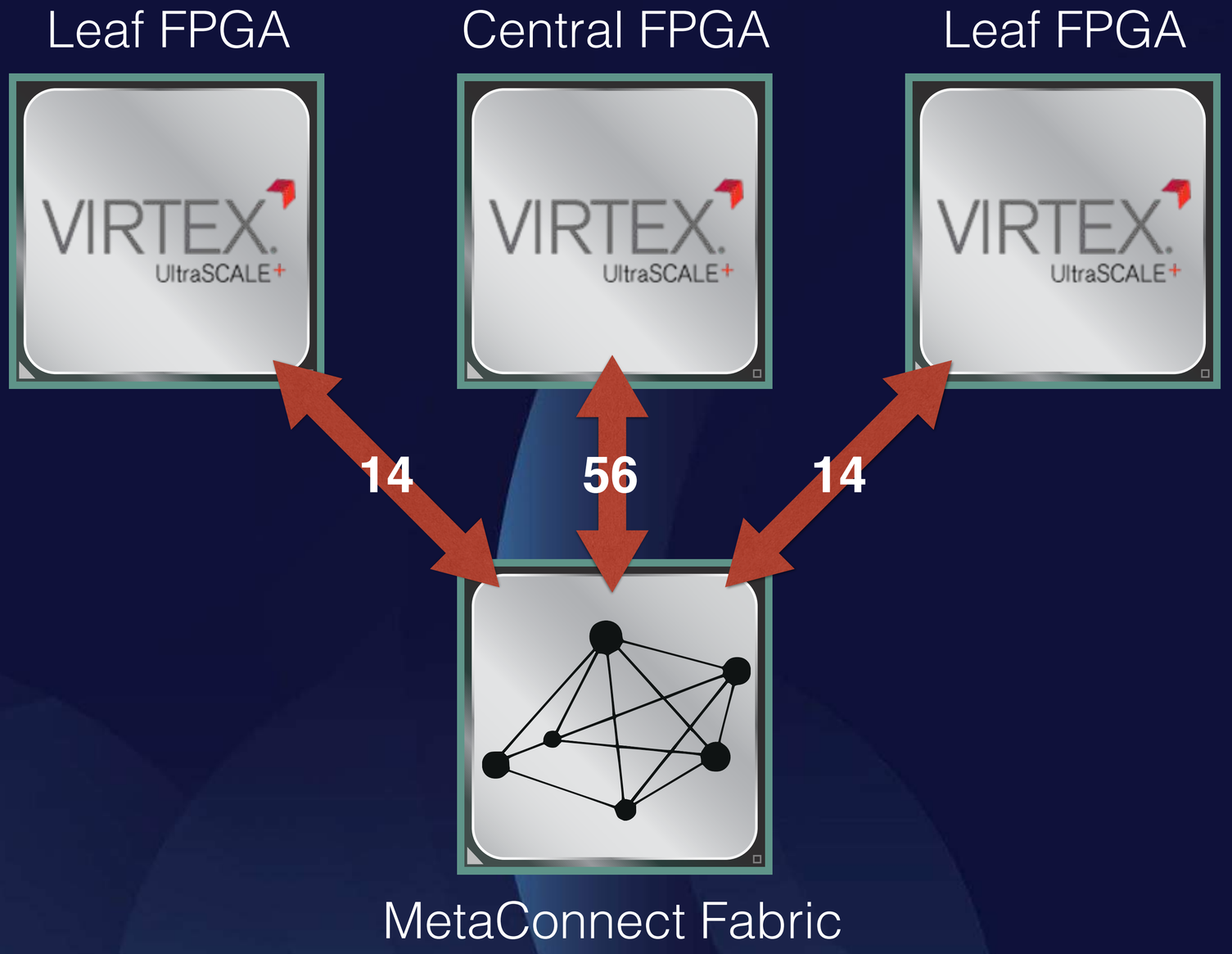
- **Ultrascale** and **Ultrascale+** FPGA
- MetaApp 32E, MetaMux 48E and MetaConnect 96E
- All include “MetaConnect”



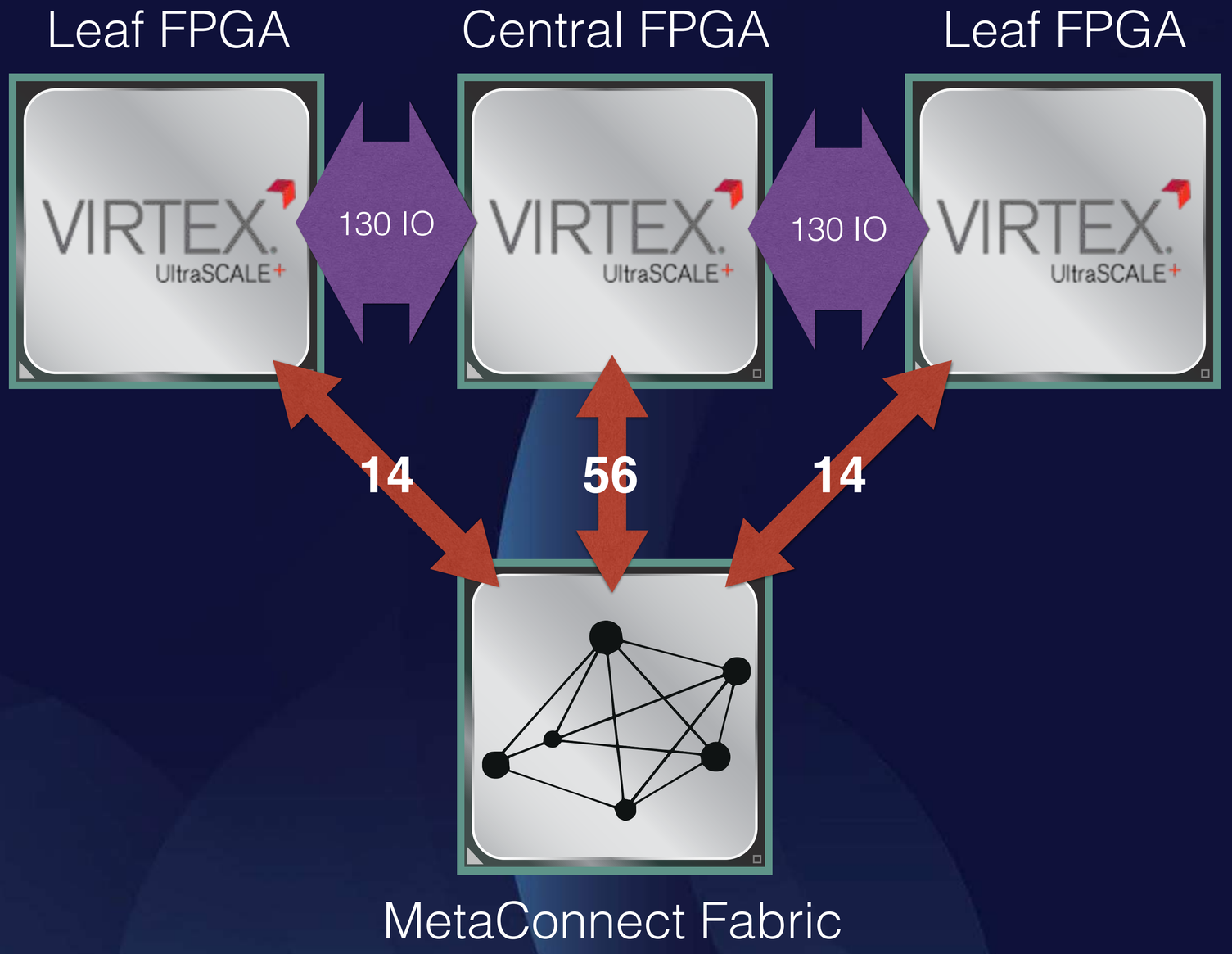
E-Series



E-Series

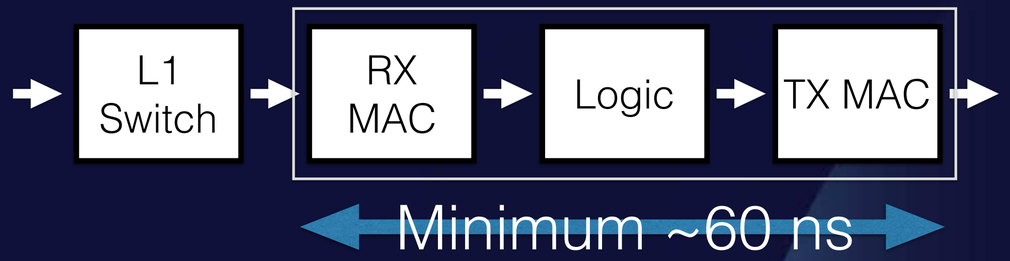

Leaf FPGA
Central FPGA
Leaf FPGA
VIRTEX
UltraSCALE+
VIRTEX
UltraSCALE+
VIRTEX
UltraSCALE+
14
56
14
MetaConnect Fabric

E-Series


Leaf FPGA
Central FPGA
Leaf FPGA
VIRTEX UltraSCALE+
130 IO
VIRTEX UltraSCALE+
130 IO
VIRTEX UltraSCALE+
14
56
14
MetaConnect Fabric

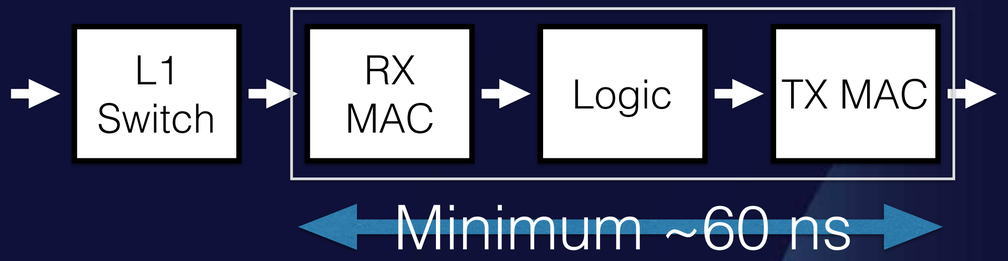
E-Series

One FPGA

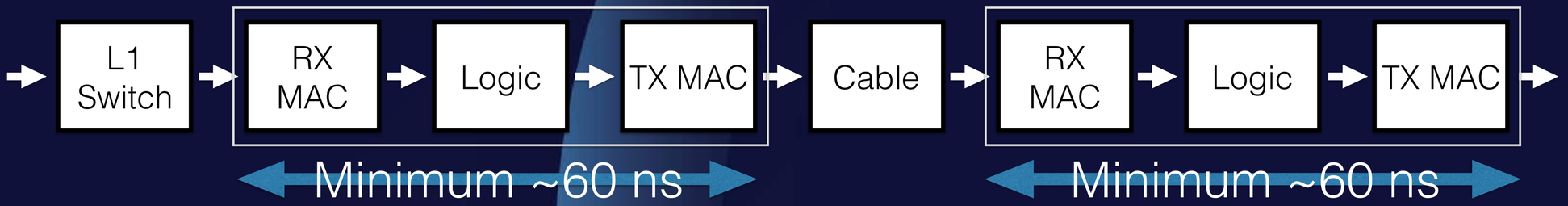


E-Series

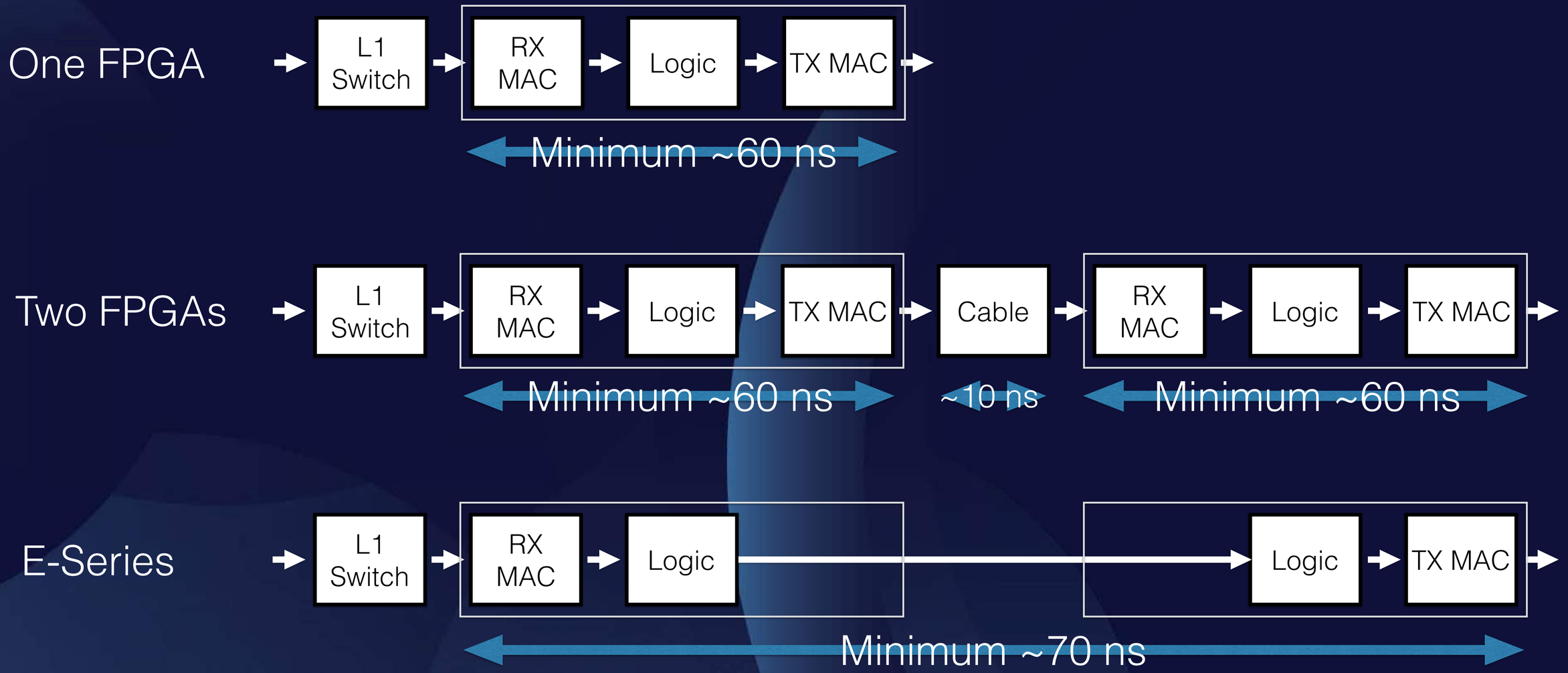
One FPGA



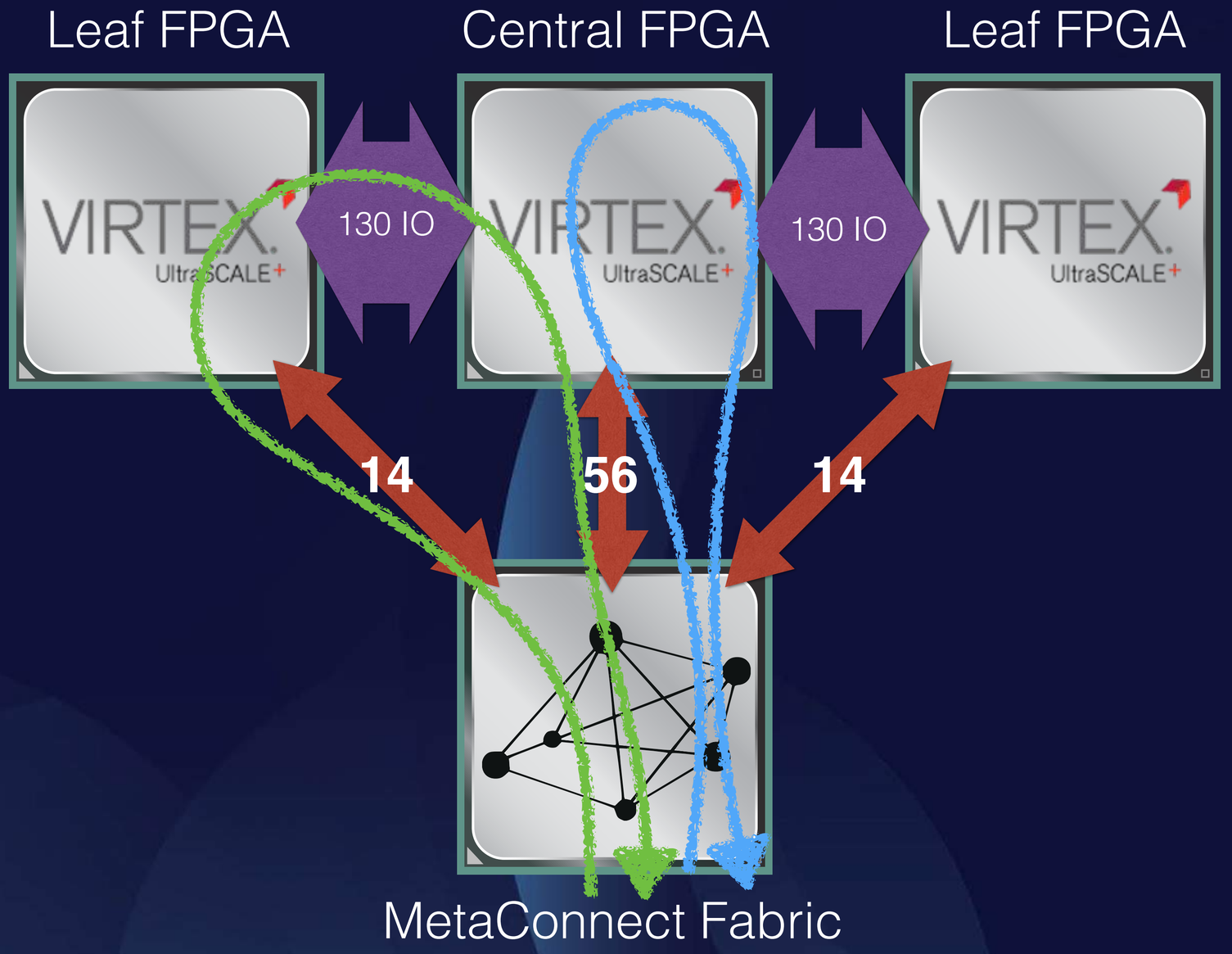
Two FPGAs



E-Series


One FPGA
L1 Switch
RX MAC
Logic
TX MAC
Minimum ~60 ns
Two FPGAs
L1 Switch
RX MAC
Logic
TX MAC
Cable
RX MAC
Logic
TX MAC
Minimum ~60 ns
~10 ns
Minimum ~60 ns
E-Series
L1 Switch
RX MAC
Logic
Logic
TX MAC
Minimum ~70 ns

E-Series

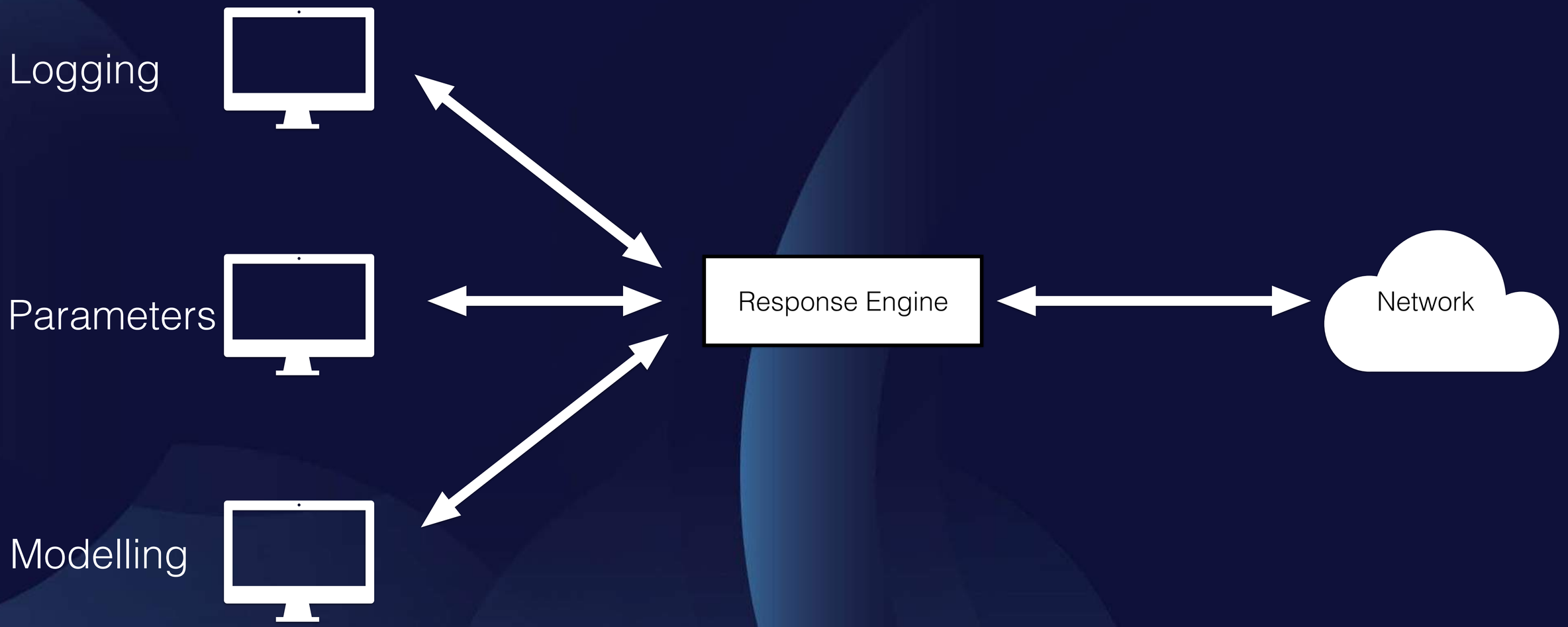

Leaf FPGA
Central FPGA
Leaf FPGA
VIRTEX
UltraSCALE+
130 IO
130 IO
14
56
14
MetaConnect Fabric

E-Series

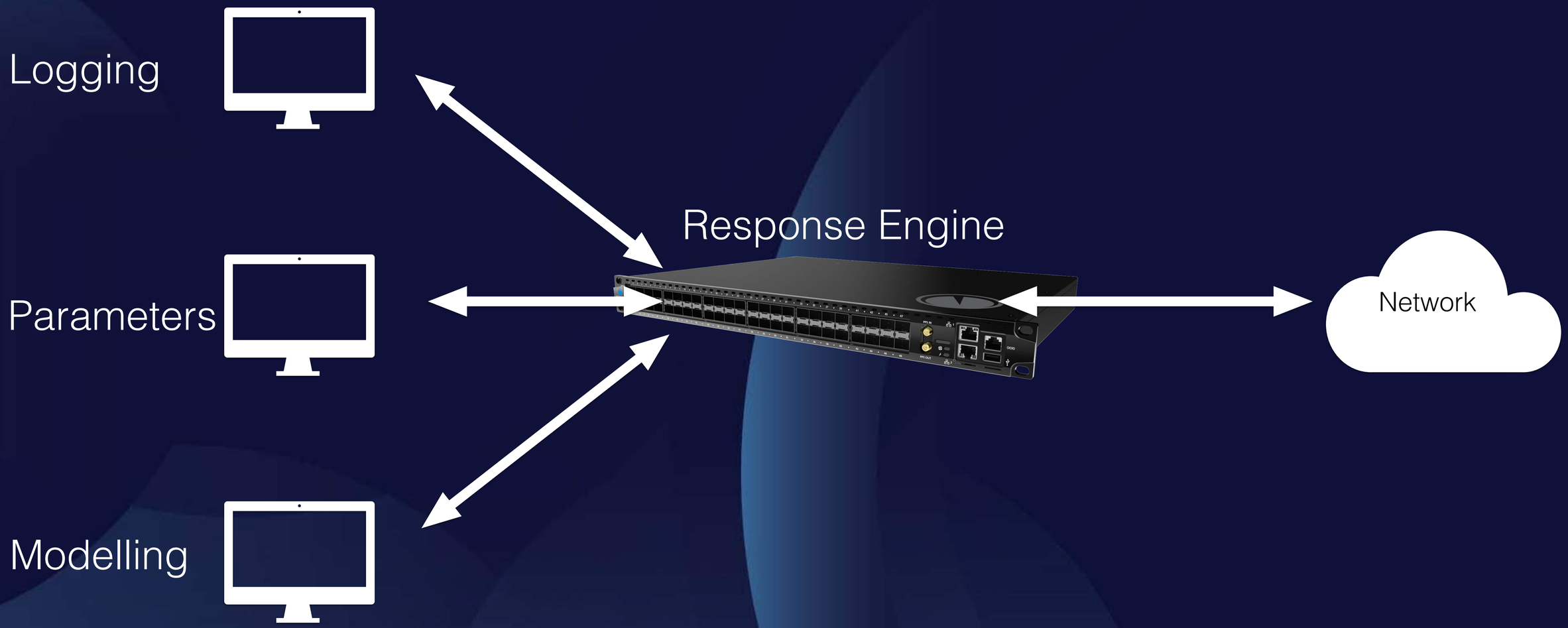
	K-Series (Virtex 7 415T)	C-Series (Arria 10)	E-Series (3x VU9P Variant)
Flip Flops or Registers	515k	1,708k	7,092k
Total On-Chip RAM	31.7 Mb	65Mb	1,037 Mb

Architectures

Architecting for the switch



Architecting for the switch



A few quick thoughts…

- Ditch PCI Express — leverage the network
- Physical distance matters
- Memory is king

Architecting for the switch

Traditional FPGA Solution

Architecting for the switch

Traditional FPGA Solution

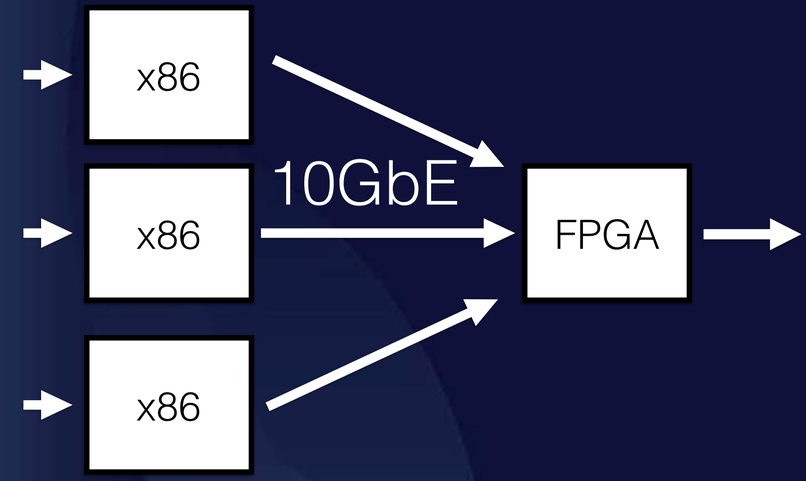
Modern FPGA Solution

Architecting for the switch

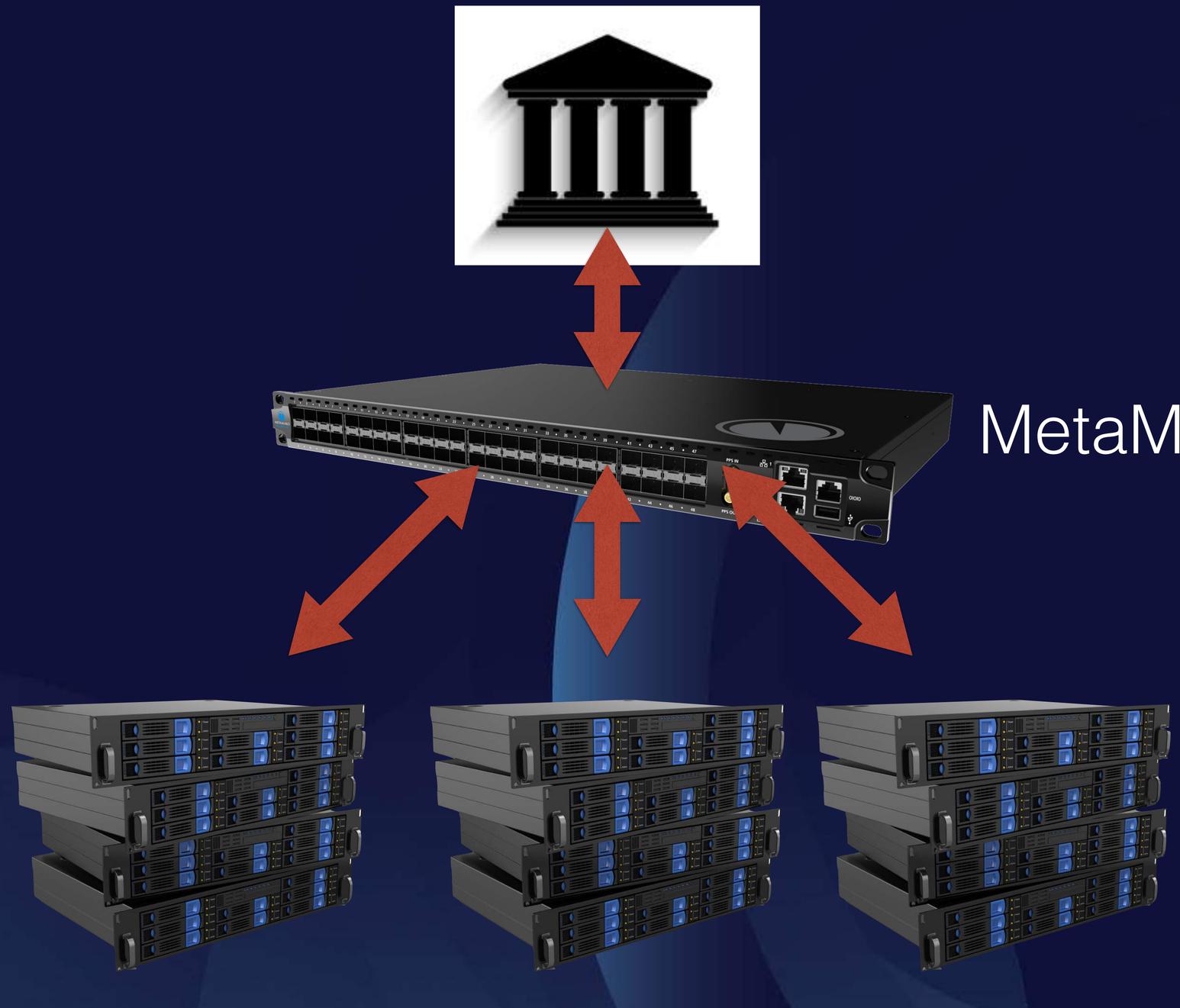
Traditional FPGA Solution

Modern FPGA Solution

Metamako FPGA Solution



E-Series



MetaMux 48E

METAMAKO

For development kits, see:

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